Remarks/Arguments

Rejections under 35 U.S.C. 103(a)

The Examiner has rejected claims 1-7, 9-26, and 33-34 under 35 U.S.C. 103(a) as being unpatentable over Kimura (U.S. Patent No. 6, 734, 553) in view of Shi *et al.* (U.S. Patent No. 7, 476, 813).

The Examiner has stated in the rejections of independent claims 1 and 17 that Kimura discloses *inter alia* an electronic apparatus comprising: "a first integrated circuit semiconductor die **40** of a first semiconductor technology"; and "a second integrated semiconductor die **50** of a second semiconductor technology physically different from the first semiconductor technology".

The Examiner stated that Kimura fails to show an ancillary circuit formed on the first integrated die for supporting operation of a signal conditioner circuit found in the second integrated die but has alleged that such is obvious by virtue of Shi *et al.*'s teaching "a multilayer flip-chip IC die package that includes various ancillary circuits" relying on Figure 1 and column 3, lines 25-40 of Shi *et al.*, and has asserted that Shi *et al.* "provides the advantage of achieving desirable impedances" relying on column 3 lines 1-5. The Examiner has alleged the motivation to combine the teachings of Shi *et al.* with Kimura is that of "achieving desirable impedances allowing a more efficient semiconductor device".

Applicant respectfully submits that Kimura does not teach a second ancillary circuit integrated within the first integrated circuit semiconductor die of a first semiconductor technology supporting a second signal conditioning circuit of a second integrated circuit semiconductor die of a second semiconductor technology physically different from the first semiconductor technology, as claimed in independent claims 1 and 17.

In the passage of Kimura relied upon by the Examiner, namely, column 4, lines 18-30, Kimura teaches that "both of the intermediate substrates 10 and 20 are formed of silicon substrate". Applicant submits that this passage describing the semiconductor technology

of the IC chips 10 and 20 as being the same is consistent with an advantage described in column 6, lines 28-35 of Kimura that "by use of *silicon substrate as the intermediate substrates*, the coefficient of thermal expansion of the intermediate substrates become *equal to that of the IC chip*". Applicant respectfully submits that by virtue of this teaching, that having the *same substrate* material is advantageous with respect to equalization of thermal expansion, Kimura *teaches away* from semiconductor technologies which are *physically different* from each other, as claimed in independent claims 1 and 17.

Applicant notes, in respect of claim 4, that the Examiner has relied on column 4, lines 52-65, of Kimura to show the feature of "the second semiconductor technology is other than silicon based technology". Applicant notes that this passage cited by the Examiner makes no mention of what material the *semiconductor technology* of Kimura is based on, merely describing the type of metal that may be used in *wires to connect various bonding pads* such as Au or Al. If this is an indication of what the Examiner interprets as the subject matter identified in the independent claims as the "second semiconductor technology", then it is clear that the Examiner is making an inappropriate application of the prior art to the claim limitations.

Furthermore, the Examiner has reasoned that the motivation to combine Kimura and Shi *et al.* to allegedly obtain the features of the independent claims, is that of a desire to achieve desirable impedances which Shi *et al.* discusses at column 3, lines 1-5. Applicant submits, however, that the Examiner has not shown any Shi et al., Kimura, or any combination thereof in the indication that using chips of different technologies, specifically using one's circuit of a 1st semiconductor technology and support for another circuit on a different semiconductor technology, has the effect of impedance matching or is particularly advantageous to achieve impedance matching. In the absence of any indication of this kind in the prior art, applicant submits that the Examiner has not shown any rational connection between the prior art and the features of the independent claims that alleged motivation provides.

Applicant respectfully submits that Kimura and Shi *et al.* singly or in combination do not disclose, teach, or suggest all of the features of each of independent claims 1 and 17, and particularly the feature of: a second ancillary circuit integrated within the first integrated circuit semiconductor die of a first semiconductor technology supporting a second signal conditioning circuit of a second integrated circuit semiconductor die of a second semiconductor technology physically different from the first semiconductor technology.

Applicant submits therefore that all the claim of the present application are not obvious in view of Kimura in further view of Shi *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 103(a) rejections of claims 1-7, 9-26, and 33-37.

Applicant submits that the present application is in allowable form and respectfully requests allowance in this case.

A Petition for Extension of Time is filed concurrently with this response.

Please charge any additional fees required or credit any overpayment to Deposit Account No. 20-1430.

Respectfully submitted,

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